WHAT IS CLAIMED IS:

1. A semiconductor component comprising:

a semiconductor die comprising a die contact;

a polymer layer on the die;

a redistribution conductor on the polymer layer in electrical communication with the die contact; and

a bonding pad on the polymer layer comprising a portion of the conductor, and a metal layer on the portion.

2. The semiconductor component of claim 1 further comprising a non-oxidizing metal layer on the metal layer.

3. The semiconductor component of claim 2 wherein the non-oxidizing metal layer comprises Au, Pt or Pd.

4. The semiconductor component of claim 2 wherein the non-oxidizing metal layer covers the bonding pad.

5. The semiconductor component of claim 2 wherein the non-oxidizing metal layer covers the conductor.

6. The semiconductor component of claim 2 wherein the semiconductor die comprises an integrated circuit in electrical communication with the die contact.

7. A semiconductor component comprising:

a semiconductor die including a circuit side and a plurality of die contacts on the circuit;

a polymer layer on the circuit side;

a plurality of redistribution conductors on the polymer layer in electrical communication with the die contacts;

a plurality of bonding pads on the polymer layer in electrical communication with the conductors, each bonding pad comprising a conductive layer, a barrier/adhesion layer and a non-oxidizing layer.

8. The semiconductor component of claim 7 further comprising a plurality of metal bumps on the die contacts, each metal bump having a same planar surface as the polymer layer.

9. The semiconductor component of claim 7 wherein each conductor comprises a portion of the conductive layer, a portion of the barrier/adhesion layer and a portion of the non-oxidizing layer.

10. The semiconductor component of claim 7 further comprising a plurality of terminal contacts on the bonding pads.

11. The semiconductor component of claim 7 wherein the die contacts have a first pattern and the bonding pads have a second pattern.

12. The semiconductor component of claim 7 wherein the conductive layer comprises a portion of a conductor.

13. The semiconductor component of claim 7 wherein the barrier/adhesion layer comprises a metal selected from the group consisting of Ni, V, Cr, CrCu and Cu.

14. The semiconductor component of claim 7 wherein the non-oxidizing layer comprises a metal selected from the group consisting of Au, Pt and Pd.

15. A semiconductor component comprising:

a semiconductor die including a plurality of integrated circuits and a plurality of die contacts in electrical communication with the circuits having a first pattern;

a polymer layer on the die;

a plurality of conductors on the polymer layer;

a plurality of bonding pads on the polymer layer in electrical communication with the conductors and having a second pattern;

the conductors and the bonding pads comprising a metal stack including a conductive layer, a barrier/adhesion layer and a non-oxidizing layer.

16. The semiconductor component of claim 15 further comprising a metal bump on each die contact embedded in the polymer layer.

17. The semiconductor component of claim 15 further comprising a second polymer layer on the conductors having openings aligned with the bonding pads.

18. The semiconductor component of claim 15 wherein the polymer layer comprises a material selected from the group consisting of polyimide, PBO, and BCB.

19. The semiconductor component of claim 15 further comprising a stud bump bonded to each bonding pad.

20. A semiconductor component comprising:

a semiconductor die including a circuit side and a plurality of die contacts on the circuit having a first pattern;

a polymer layer on the circuit side;

a plurality of conductors on the polymer layer in electrical communication with the die contacts; and

a plurality of bonding pads on the conductors having a second pattern;

each conductor and each bonding pad comprising a conductive layer, a barrier/adhesion layer and a non-oxidizing layer.

21. The semiconductor component of claim 20 wherein the conductors have a thickness determined by the barrier/adhesion layer and the non-oxidizing layer, the thickness selected to achieve desired electrical for the conductors.

22. The semiconductor component of claim 20 further comprising a second polymer layer on the circuit side encapsulating the conductors and having a plurality of openings aligned with the bonding pads.

23. The semiconductor component of claim 20 wherein the non-oxidizing layer completely seals the conductors and the bonding pads.

24. The semiconductor component of claim 20 wherein the barrier/adhesion layer comprises Ni.

25. The semiconductor component of claim 20 wherein the non-oxidizing layer comprises gold.

26. The semiconductor component of claim 20 further comprising a plurality of stud bumps on the bonding pads.

27. The semiconductor component of claim 20 wherein the die contacts comprise bond pads.

28. The semiconductor component of claim 20 further comprising a plurality of wires wire bonded to the bonding pads.

29. A method for fabricating a semiconductor component comprising:

providing a semiconductor die comprising a die contact;

forming a polymer layer on the die;

forming a redistribution conductor on the polymer layer in electrical communication with the die contact;

forming a bonding pad on the conductor;

forming a first metal layer on the bonding pad; and

forming a non-oxidizing metal layer on the first metal layer.

30. The method of claim 29 wherein the non-oxidizing metal layer comprises Au, Pt or Pd.

31. The method of claim 29 wherein the first metal layer comprises a metal selected from the group consisting of Ni V, Cr, CrCu and Cu.

32. The method of claim 29 wherein the non-oxidizing metal layer covers the bonding pad and the conductor.

33. The method of claim 29 further comprising forming a stud bump on the bonding pad.

34. The method of claim 29 further comprising wire bonding a wire to the bonding pad.

35. The method of claim 29 further comprising forming a second polymer layer on the die and the conductor having an opening aligned with the bonding pad.

36. A method for fabricating a semiconductor component comprising:

providing a die comprising a circuit side and a plurality of die contacts on the circuit side having a first pattern;

forming a polymer layer on the circuit side;

forming a plurality of conductors on the polymer layer in electrical communication with the die contacts;

forming a plurality of bonding pads on the polymer layer in electrical communication with the conductors and having a second pattern;

forming a barrier/adhesion layer on the conductors and the bonding pads; and

forming a non-oxidizing layer on the barrier/adhesion layer.

37. The method of claim 36 wherein the forming the conductors step and the forming the bonding pads step comprise electrolessly depositing a first metal.

38. The method of claim 36 wherein the forming the barrier/adhesion layer step comprises electrolessly depositing a second metal.

39. The method of claim 36 wherein the forming the non-oxidizing layer step comprises electrolessly depositing a third metal.

40. The method of claim 36 wherein the polymer layer comprises a material selected from the group consisting of polyimide, PBO and BCB.

41. The method of claim 36 wherein the barrier/adhesion layer comprises a material selected from the group consisting of a metal selected from the group consisting of V, Cr, CrCu and Cu.

42. A method for fabricating a semiconductor component comprising:

providing a substrate comprising a semiconductor die comprising a plurality of die contacts;

forming a plurality of metal bumps on the die contacts;

forming a polymer layer on the die and planarizing the polymer layer and the metal bumps to a same surface;

forming a plurality of conductors on the polymer layer in electrical communication with the metal bumps, the conductors comprising bonding pads having a different pattern than the die contacts;

forming a barrier/adhesion layer on the conductors and the bonding pads;

forming a non-oxidizing layer on the barrier/adhesion layer; and

singulating the die from the substrate.

43. The method of claim 42 further comprising forming a plurality of stud bumps on the bonding pads.

44. The method of claim 42 further comprising forming a plurality of wire bonds on the bonding pads.

45. The method of claim 42 further comprising forming a second polymer layer on the die having openings aligned with the bonding pads.

46. The method of claim 42 wherein the substrate comprises a semiconductor wafer.

47. The method of claim 42 wherein the forming the barrier/adhesion layer step comprises electrolessly depositing Ni.

48. The method of claim 42 wherein the forming the non-oxidizing layer step comprises electrolessly depositing Au.

49. A method for fabricating a semiconductor component comprising:

providing a semiconductor die including a circuit side and a plurality of die contacts on the circuit having a first pattern;

forming a polymer layer on the circuit side;

forming a plurality of conductors on the polymer layer in electrical communication with the die contacts; and

forming a plurality of bonding pads on the conductors having a second pattern;

forming a barrier/adhesion layer on the conductors and the bonding pads; and

forming a non-oxidizing layer on the barrier/adhesion layer.

50. The method of claim 49 further comprising adjusting electrical characteristics of the conductors by controlling a thickness of the barrier/adhesion layer.

51. The method of claim 49 further comprising forming a second polymer layer on the circuit side encapsulating the conductors and having a plurality of openings aligned with the bonding pads.

52. The method of claim 49 wherein the non-oxidizing layer completely seals the conductors and the bonding pads.

53. The method of claim 49 further comprising forming a plurality of stud bumps on the bonding pads.

54. The method of claim 53 further comprising wire bonding to the stud bumps.

55. The method of claim 49 further comprising wire bonding to the bonding pads.

56. An electronic assembly comprising:

a supporting substrate comprising an electrode;

a semiconductor component on the substrate comprising a semiconductor die having a die contact, a polymer layer on the die, a redistribution conductor on the polymer layer in electrical communication with the die contact, and a bonding pad on the polymer layer comprising a portion of the conductor, a metal layer on the portion and a non-oxidizing metal on the metal layer; and

a wire bonded to the electrode and to the bonding pad.

57. The electronic assembly of claim 56 wherein the substrate comprises a module substrate, a package substrate or a printed circuit board.

58. The electronic assembly of claim 56 wherein the non-oxidizing metal comprises Au, Pt or Pd.

59. The electronic assembly of claim 56 wherein the metal layer comprises a metal selected from the group consisting of Ni, V, Cr, CrCu and Cu.

60. The electronic assembly of claim 56 wherein the semiconductor die comprises an integrated circuit in electrical communication with the die contact.

61. An electronic assembly comprising:

a supporting substrate;

an interposer on the supporting substrate comprising a polymer layer, a plurality of conductors on the polymer layer, and a plurality of bonding pads on the conductors, each bonding pad comprising a barrier/adhesion metal layer and a non-oxidizing metal layer; and

a semiconductor die on the interposer comprising a plurality of die contacts wire boned to the bonding pads.

62. The electronic assembly of claim 61 wherein the supporting substrate comprises a second semiconductor die.

63. The electronic assembly of claim 61 wherein the interposer has a smaller footprint than the supporting substrate and the semiconductor die has a smaller footprint than the interposer.

64. An electronic assembly comprising

a semiconductor die comprising a plurality of die contacts having a first pattern, a polymer layer, a plurality of conductors on the polymer layer in electrical communication with the die contacts, and a plurality of

bonding pads on the conductors having a second pattern, each conductor and each bonding pad comprising a conductive layer, a barrier/adhesion layer and a non-oxidizing layer; and

a plurality of lead fingers attached to the die and wire bonded to the bonding pads.

65. The electronic assembly of claim 64 further comprising a plastic body encapsulating the die and a portion of the lead fingers.

66. The electronic assembly of claim 64 wherein the die is attached to the lead fingers in a lead on chip configuration.

67. The electronic assembly of claim 64 wherein the bonding adhesion/layer comprises Ni, V, Cr, CrCu or Cu.

68. The electronic assembly of claim 64 wherein the non-oxidizing layer comprises Au, Pt or Pd.